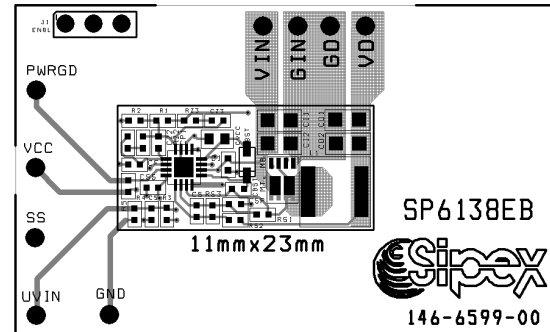
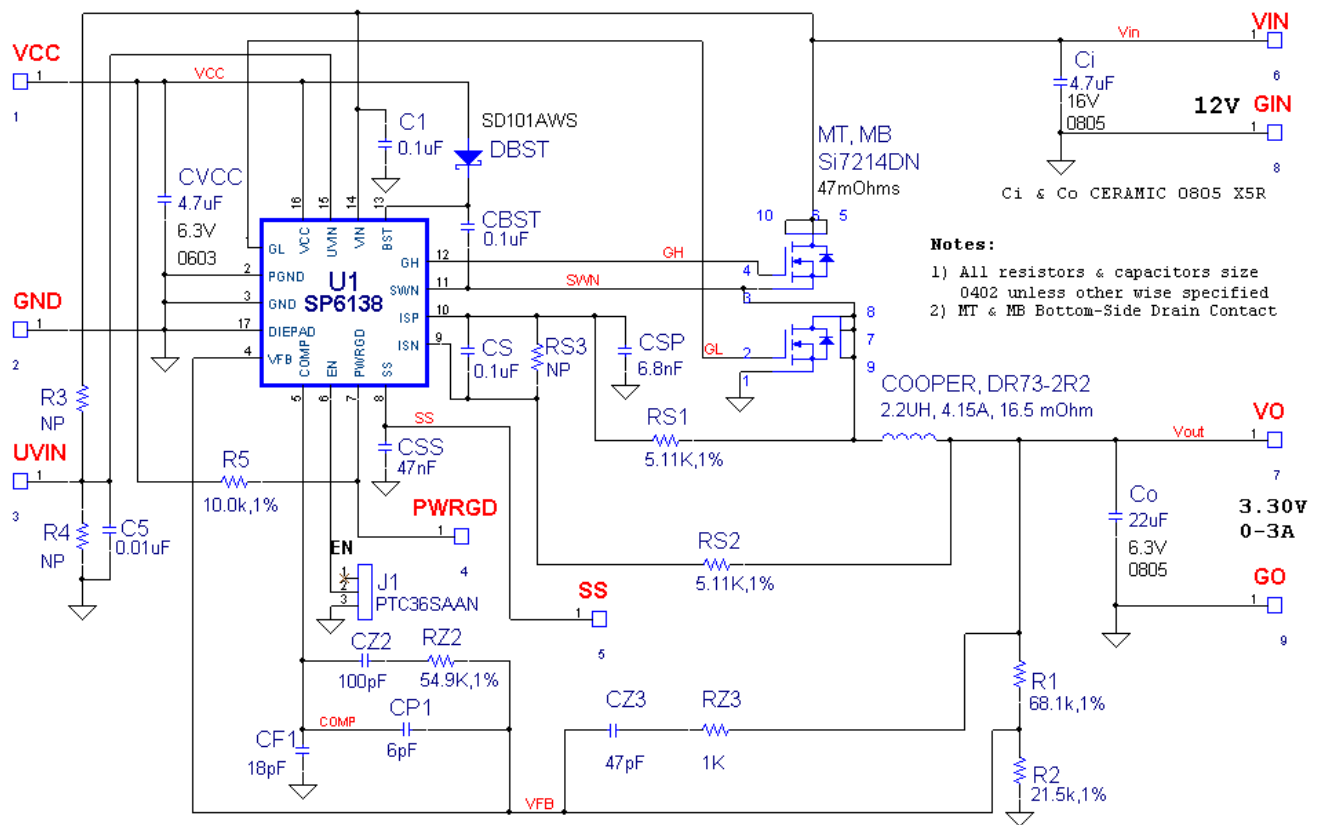


- Easy Evaluation for the SP6138ER1 12V Input, 0 to 3A Output Synchronous Buck Converter
- Precision 0.80V with $\pm 1\%$ High Accuracy Reference
- Small form factor
- Feature Rich: Single supply operation, Over-current protection with auto-restart, Power Good Output, Enable input, Fast transient response, Supply and Output Dead Short Circuit Shutdown Protection, Programmable soft start.



SP6138EB SCHEMATIC



USING THE EVALUATION BOARD

1) Powering Up the SP6138EB Circuit

Connect the SP6138 Evaluation Board with an external +12V power supply. Connect with short leads and large diameter wire directly to the “VIN” and “GIN” posts. Connect a Load between the “Vo” and “Go” posts, again using short leads with large diameter wire to minimize inductance and voltage drops.

2) Measuring Output Load Characteristics

It's best to ground any reference scope and digital meters using the Star GND post in the center of the board. V_{OUT} ripple can best be seen by touching the probe tip to the pad for C_{OUT} and the scope GND collar touching the Star GND post – avoid a GND lead on the scope which will increase noise pickup.

3) Using the Evaluation Board with Different Output Voltages

The SP6138 Evaluation Board has been tested and delivered with the output set to 3.30V. By simply changing one resistor, R₂, the SP6138 can be set to other output voltages. The relationship in the following formula is based on a voltage divider from the output to the feedback pin V_{FB}, which is set to an internal reference voltage of 0.80V. Standard 1% metal film resistors of surface mount size 0603 are recommended.

$$V_{OUT} = 0.80V (R_1 / R_2 + 1) \Rightarrow R_2 = R_1 / [(V_{OUT} / 0.80V) - 1]$$

Where R₁ = 68.1KΩ and for the V_{OUT} = 0.80V setting, simply remove R₂ from the board. Furthermore, one could select the value of R₁ & R₂ combination to meet the exact output voltage setting by restricting R₁ resistance range such that 50KΩ ≤ R₁ ≤ 100KΩ for overall system loop stability.

Note that since the SP6138 Evaluation Board design was optimized for 12V down conversion to 3.30V, changes of output voltage and/or input voltage will alter performance from the data given in the Power Supply Data section.

POWER SUPPLY DATA

The SP6138EB is designed with an accurate 1.5% reference over line, load and temperature. Figure 1 data shows a typical SP6138ER Evaluation Board efficiency plot, with efficiencies to 86% and output currents to 3A. SP6138ER Load Regulation in Figure 2 shows only 0.09% change in output voltage step response from no load to 3A load. Figures 3 and 4 show the fast transient response of the SP6138. Start-up response in Figures 5, 6 and 7 show a controlled start-up with different output load behavior when power is applied where the input current rises smoothly as the soft-start ramp increases. In Figure 8 the hiccup mode gets activated in response to an output dead short circuit condition and will soft-start until the over-load is removed. Figures 9 and 10 show output voltage ripple less than 10mV over the complete load range.

While data on individual power supply boards may vary, the capability of the SP6138ER of achieving high accuracy over a range of load conditions shown here is quite impressive and desirable for accurate power supply design.

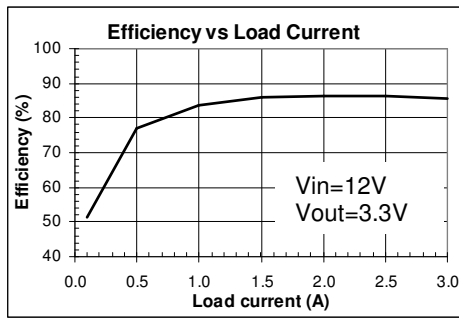


Figure 1. Efficiency vs Load

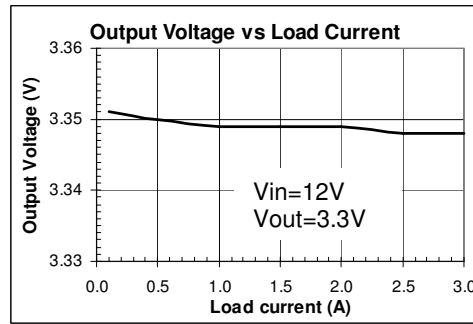


Figure 2. Load Regulation

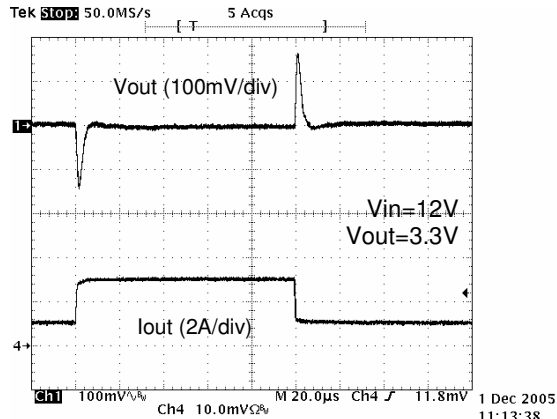


Figure 3. Load Step Response: 1->3A

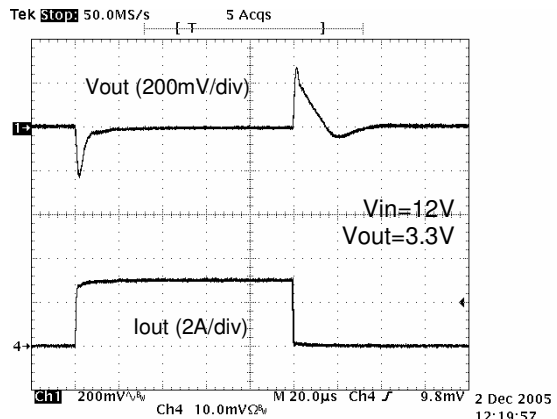


Figure 4. Load Step Response: 0->3A

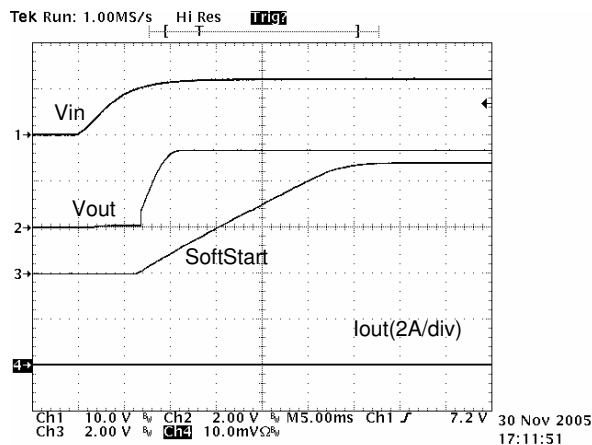


Figure 5. Start-Up Response: No Load Load

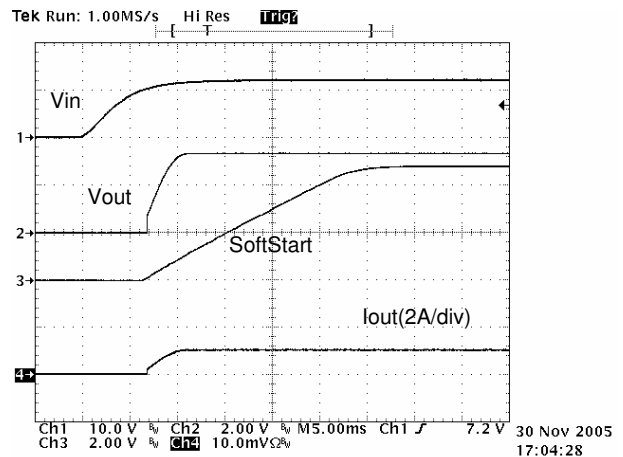


Figure 6. Start-Up Response: 1A

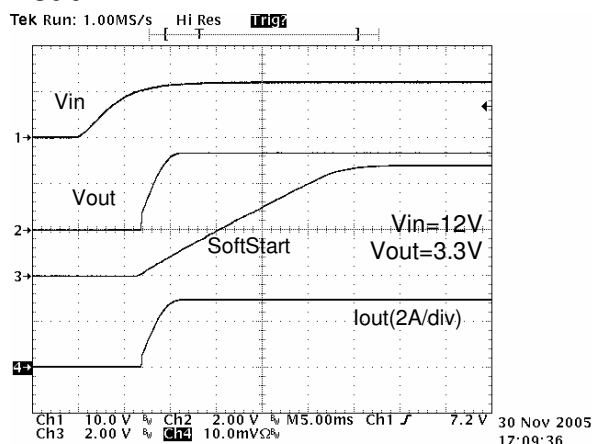


Figure 7. Start-Up Response: 3A Load

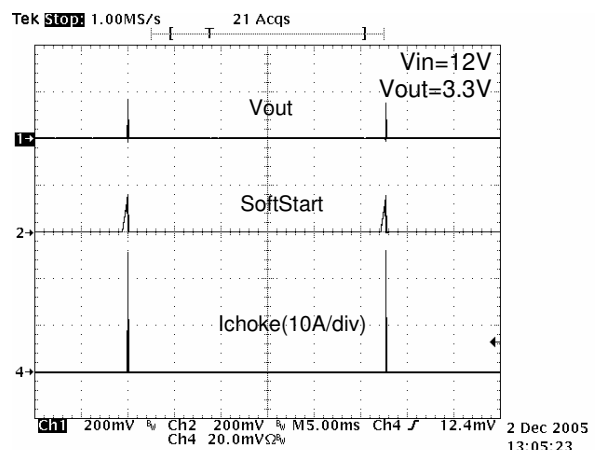


Figure 8. Output Load Short Circuit

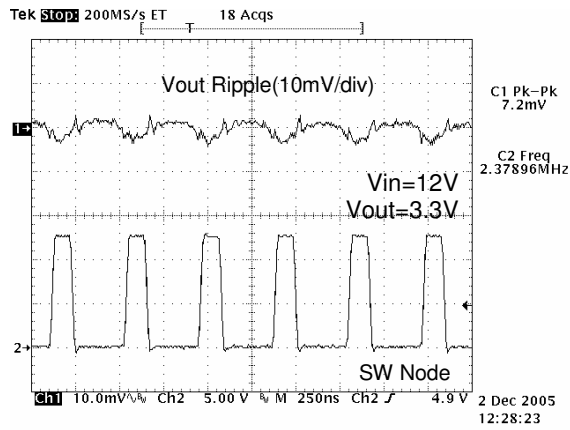


Figure 9. Output Noise at No Load

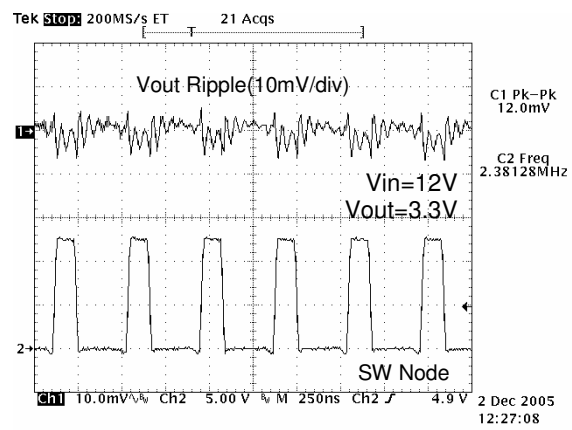


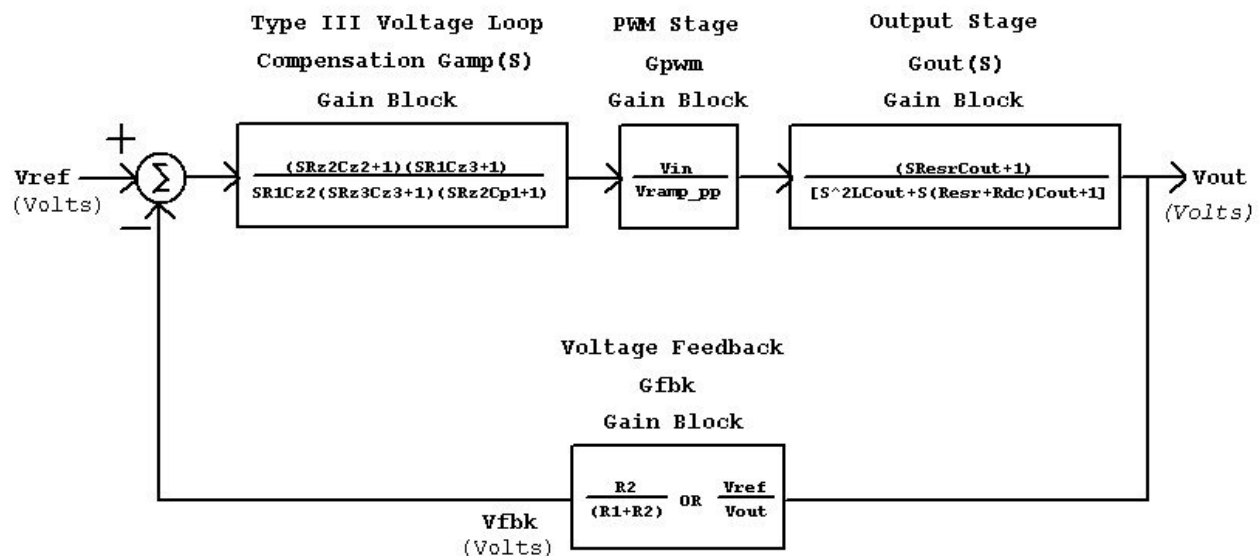
Figure 10. Output Noise at 3A Load

INDUCTORS - SURFACE MOUNT								
Inductance (uH)	Manufacturer/Part No.	Inductor Specification				Inductor Type	Manufacturer Website	
		Series R (mOhms)	Isat (A)	Size (LxW(mm) Ht.(mm))				
2.2	COOPER DR73-2F2	16.5	5.52	7.6X6.0	3.55	Shielded Ferrite Core	www.cooperet.com	
CAPACITORS - SURFACE MOUNT								
Capacitance (uF)	Manufacturer/Part No.	Capacitor Specification					Capacitor Type	Manufacturer Website
		ESR (ohms (max))	Ripple Current (A) @45C	Size (LxW(mm) Ht.(mm))		Voltage (V)		
4.7	AVX 08053D475MAT	0.005	4.00	2.0x1.25	1.25	16.0	X5R Ceramic	www.avx.com
22	AVX 08056D226MAT	0.005	4.00	2.0x1.25	1.25	6.3	X5R Ceramic	www.avx.com
MOSFETS - SURFACE MOUNT								
MOSFET	Manufacturer/Part No.	MOSFET Specification					Foot Print	Manufacturer Website
		RDS(on) (ohms (max))	ID Current (A)	Cg (nC (Typ) nC (Max))		Voltage (V)		
Dual N-Ch	VISHAY SI7214DN	0.047	5.9	4.2	6.5	30.0	Power-PAK 1212-8	www.vishay.com

Table 1: SP6138EB Suggested Components and Vendor Lists

LOOP COMPENSATION DESIGN

The open loop gain of the SP6138 Evaluation Board can be divided into the gain of the error amplifier **GAMP(s)**, PWM modulator **GPWM**, buck converter output stage **GOUT(s)**, and feedback resistor divider **GFBK**. In order to crossover at the selected frequency **fco**, the gain of the error amplifier must compensate for the attenuation caused by the rest of the loop at this frequency. The goal of loop compensation is to manipulate the open loop frequency response such that its gain crosses over 0dB at a slope of -20dB/dec. The open loop crossover frequency should be higher than the ESR zero of the output capacitors but less than 1/5 of the switching frequency **fs** to insure proper operation. Since the SP6138EB is designed with ceramic type output capacitors, a Type III compensation circuit is required to give a phase boost of 180° in order to counteract the effects of the output **LC** underdamped resonance double pole frequency.



Definitions:

Resr := Output Capacitor Equivalent Series Resitance

Rdc := Output Inductor DC Resistance

Vramp_pp := SP6134 Internal RAMP Amplitude Peak to Peak Voltage

Conditions:

$Cz2 \gg Cp1$ and $R1 \gg Rz3$

Output Load Resistance \gg Resr and Rdc

Figure 11. SP6138EB Voltage Mode Control Loop with Loop Dynamic

The simple guidelines for positioning the poles and zeros and for calculating the component values for a Type III compensation scheme are as follows:

$$R1 = 68.1K$$

$$R2 = \frac{0.8 \cdot R1}{V_{out} - 0.8} \quad (\text{sets output voltage})$$

$$C_{Z3} = \frac{1}{ZSF \cdot \frac{1}{\sqrt{LC}} \cdot R1} \quad (\text{sets first zero})$$

$$R_{Z2} = \frac{(6.28 \cdot f_{crsover})^2 \cdot L \cdot C_{out} + 1}{6.28 \cdot f_{crsover} \cdot C_{Z3}} \cdot \frac{V_{ramp}}{V_{in}} \quad (\text{sets bandwidth})$$

$$C_{Z2} = \frac{1}{ZSF \cdot \frac{1}{\sqrt{LC}} \cdot R_{Z2}} \quad (\text{sets second zero})$$

$$C_{P1} = \frac{1}{6.28 \cdot f_{sw} \cdot R_{Z2}} \quad (\text{sets first high frequency pole})$$

$$R_{Z3} = \frac{1}{6.28 \cdot f_{sw} \cdot C_{Z3}} \quad (\text{sets second high frequency pole})$$

Where $ZSF = (f \text{ compensation double zero}) / (f \text{ circuit double pole})$

Here ZSF is set at 1.2.

As a particular example, consider for the following SP6138EB, 3A_{MAX} with a type III Voltage Loop Compensation component selections:

$V_{in_max} = 15V$

$V_{out} = 3.30V @ 0 \text{ to } 3A \text{ load}$

Select $L = 2.2 \mu H \Rightarrow 15\% \text{ current ripple.}$

Select $C_{out} = 22\mu F$ Ceramic capacitors ($R_{esr} \approx 5m\Omega$)

$f_s = 2500KHz$ SP6138ER1 internal Oscillator Frequency

$V_{ramp_pp} = 1.0V$ SP6138ER1 internal Ramp Peak-to-Peak Amplitude

Step by step design procedures:

- a. **R2** = 21.8 Ω
- b. **CZ3** = 85pF
- c. **Let fcrsover=200KHz then:**
- d. **RZ2** = 60.3k Ω
- e. **CZ2** = 96pF
- f. **CP1** = 1.1pF
- g. **RZ3** = 0.75K Ω
- h. **CF1** = 18pF to stabilize SP6138ER1 internal Error Amplify

The above component values were used as a starting point for compensating the converter and after laboratory testing the values shown in the circuit schematic of page 1 were used for optimum operation.

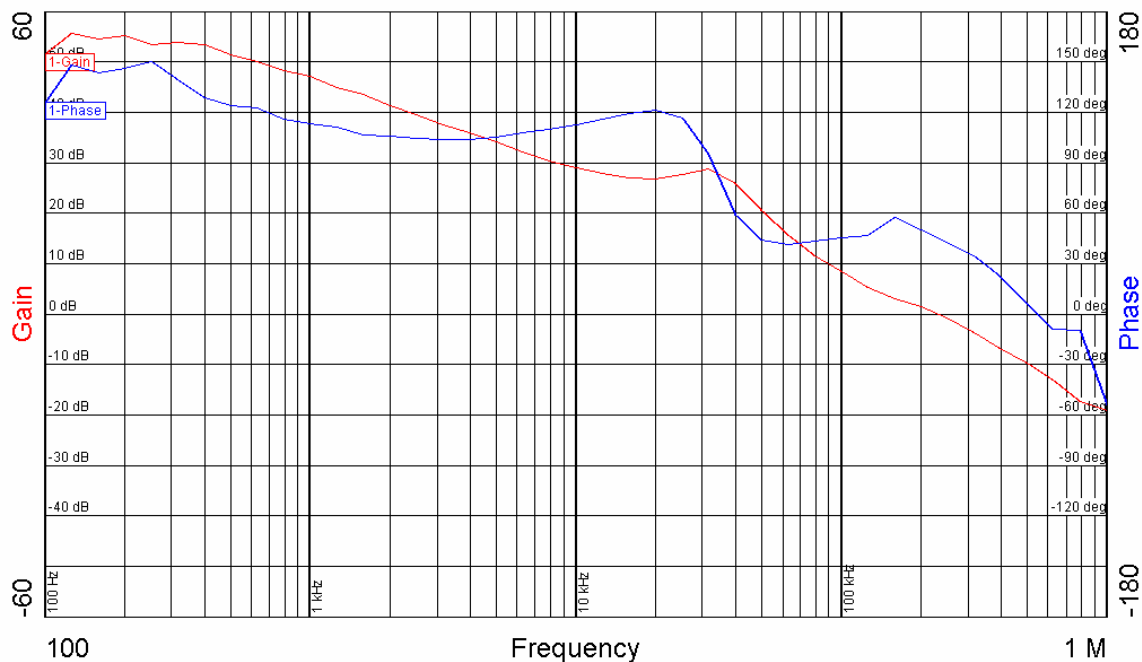


Figure 12- Gain/Phase measurement of SP6138EB shown on page 1, cross-over frequency (f_c) is just above 200KHz with a corresponding phase of 45 degrees

PCB LAYOUT DRAWINGS

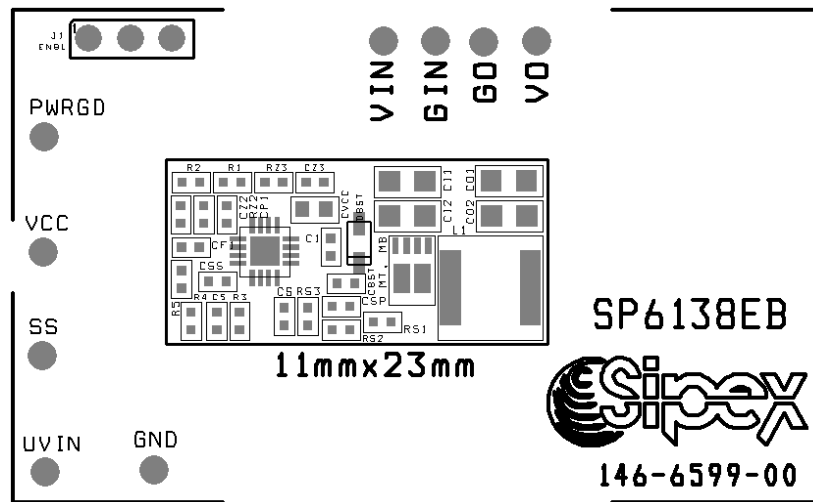


Figure 13. SP6138EB Component Placement

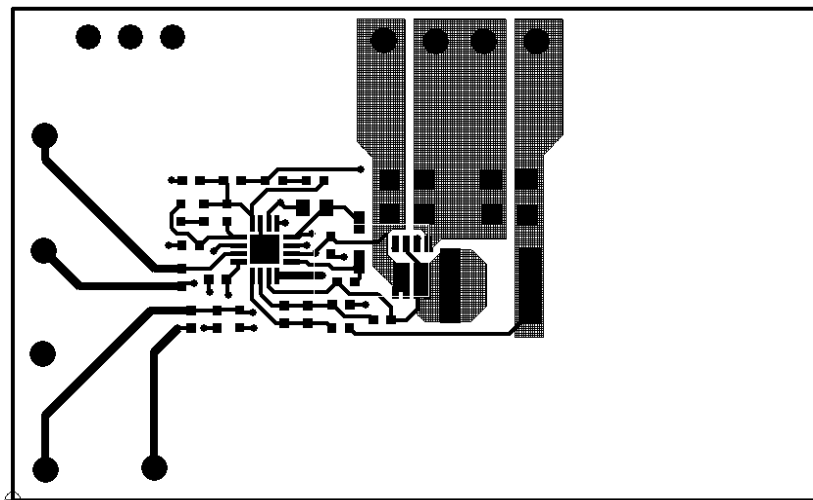


Figure 14. SP6138EB PCB Layout Top Side

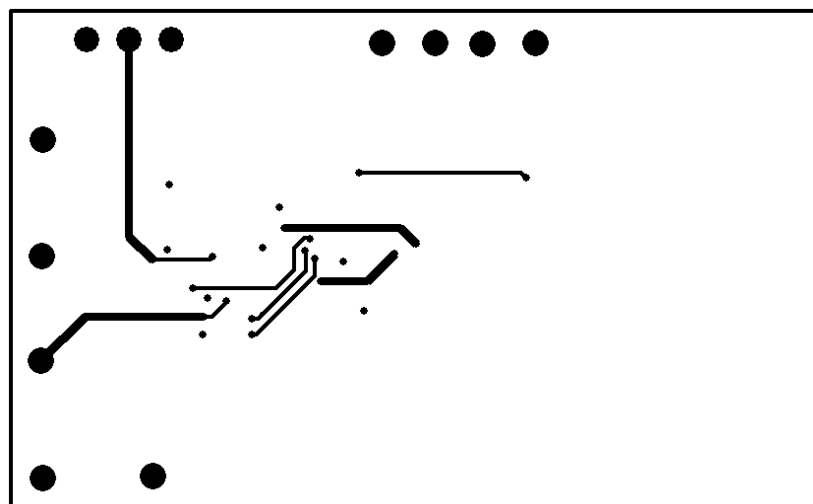


Figure 15. SP6138EB PCB Layout Bottom Side

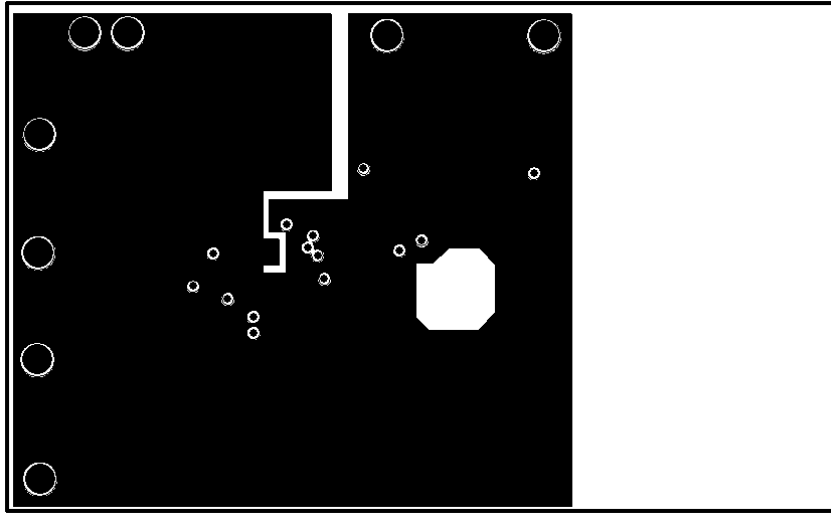


Figure 16. SP6138EB PCB Layout Inner Layer 1 & Inner Layer 2

Line No.	Ref. Des.	Qty.	Manuf.	Manuf. Part Number	Layout Size	Component	Vendor Phone Number
1	PCB	1	Sipex	146-6599-00	1.175"x1.934"	SP6138EB	978-667-7800
2	U1	1	Sipex	SP6138ER1	QFN-16	2.5MHz Synchronous Buck Controller	978-667-7800
3	MT,MB	1	Vishay Semi	Si7214DN	PowerPAK 1212-8 Dual	Dual NFET 30V, 47mOhm	402-563-6866
4	DBST	1	Vishay Semi	SD101AWS	SOD-323	15mA-30V Schottky Diode	800-344-4539
5	L1	1	COOPER Bussmann	DR73-2R2	7.6x6mm	2.20uH Coil 4.15A 16.5mOhm	561-752-5000
6	C1, CBST, CS	3	TDK	C1005JB1C104K	0402	0.1 uF Ceramic X5R 16V	978-779-3111
7	CSP	1	TDK	C1005JB1H682K	0402	6.8nF Ceramic X5R 50V	978-779-3111
8	CI	1	AVX	08053D475MAT	0805	4.7uF Ceramic X5R 25V 20%	843-448-9411
9	CO	1	AVX	08056D226MAT	0805	22uF Ceramic X5R 6.3V 20%	843-448-9411
10	CVCC	1	TDK	C1608JF0J475Z	0603	4.7uF Ceramic X5R 6.3V	978-779-3111
11	C5	1	TDK	C1005JB1E103K	0402	0.01uF Ceramic X7R 25V	978-779-3111
12	CSS	1	TDK	C1005JB1E473K	0402	47nF Ceramic X7R 25V	978-779-3111
13	CP1	1	TDK	C1005CH1H060D	0402	6pF Ceramic COG 50V 5%	978-779-3111
14	CF1	1	TDK	C1005CH1H180J	0402	18pF Ceramic COG 50V 5%	978-779-3111
15	CZ2	1	TDK	C1005CH1H101J	0402	100pF Ceramic COG 25V 5%	978-779-3111
16	CZ3	1	TDK	C1005CH1H470J	0402	47pF Ceramic COG 50V 5%	978-779-3111
17	R1	1	Panasonic	ERJ-2RKF6812X	0402	68.1K Ohm Thick Film Res 1%	800-344-4539
18	R2	1	Panasonic	ERJ-2RKF2152X	0402	21.5K Ohm Thick Film Res 1%	800-344-4539
19	R3, R4, RS3		Not populated				
20	R5	1	Panasonic	ERJ-2RKF1002X	0402	10.0K Ohm Thick Film Res 1%	800-344-4539
21	RZ2	1	Panasonic	ERJ-2RKF5492X	0402	54.9K Ohm Thick Film Res 1%	800-344-4540
22	RZ3	3	Panasonic	ERJ-2RKF1001X	0402	1.0K Ohm Thick Film Res 1%	800-344-4540
23	RS1, RS2	1	Panasonic	ERJ-2RKF4991X	0402	5.11K Ohm Thick Film Res 1%	800-344-4541
24	J1	1	Sullins	PTC36SAAN	.32x.12	36-Pin (3x12) Header	800-344-4539
25	(J1)	1	Sullins	STC02SYAN	.2x.1	Shunt	800-344-4539
26	VIN, VOUT, VCC, GIN, GO, GND, SS, PWRGD, UVIN	9	Vector Electronic	K24C/M	.042 Dia	Test Point Post	800-344-4539

Table 2: SP6138EB List of Materials

ORDERING INFORMATION

Model	Temperature Range	Package Type
SP6138EB	- 40°C to +85°C.....	SP6138 Evaluation Board
SP6138ER1.....	- 40°C to +85°C.....	16-pin QFN